MCDP52x0

USB Type-C/DisplayPort1.4a to DP++/HDMI2.0b Protocol Converter

MCDP52x0 Features

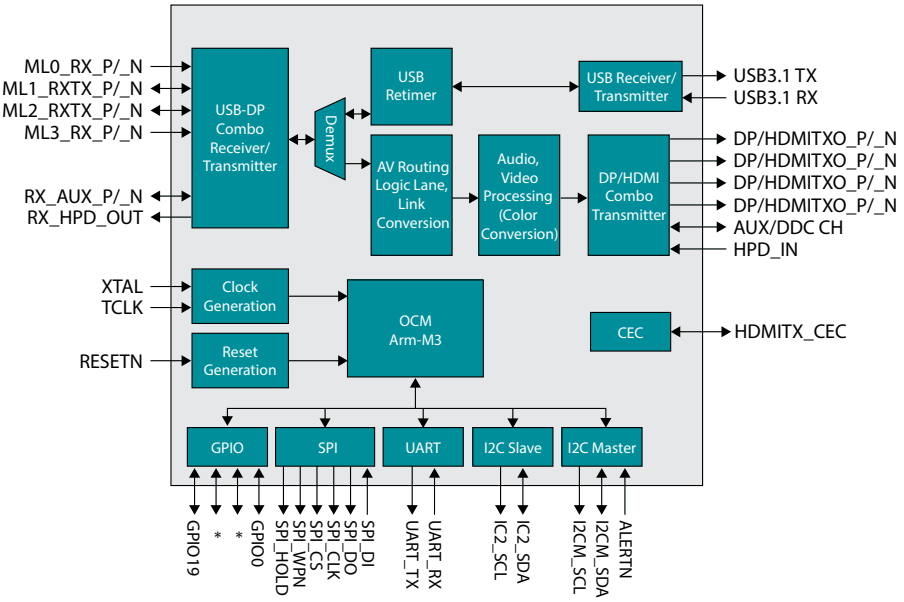
- USB Type-C "Alt mode" Receiver
- DisplayPort® (DP) ver.1.4a Compliant Receiver
- Link Rate 1.62/2.7/5.4/8.1Gbps
- USB3.1 ESS Gen1/Gen2 Retimer: 5.0 Gbps/10.0 Gbps Pairs
- DP++ TX Configurable as DP1.4a or HDMI2.0b
- HDR Image Processing (Static and Dynamic HDR)
- Adaptive Sync Support
- CEC Tunneling Over AUX
- HDCP1.x/2.x Repeater with Embedded Keys
- Package: 169 TFBGA, 7x7mm

Applications

- Notebooks and Tablets
- Adapters (dongles), Docking Stations and other AV Accessories
- Inside-the-box Applications:
  - TVs
  - Signage Game Consoles
- Advanced Driver Assistance Systems (ADAS)
- Automotive Infotainment

The MCDP52x0 is an advanced USB Type-C/DisplayPort1.4a to DP++ converter with an integrated USB type-C de-multiplexer, targeted primarily for Mobile Notebook accessory and display applications. This device functions as a DP to DP re-timer with lane count, link rate conversion option and DP to HDMI protocol converter with an HDCP1.x/ HDCP2.x repeater function.

The MCDP52x0 has a DP alt-mode capable USB Type-C Upstream Facing Port (UFP). The four high speed lanes of UFP can receive DP1.4a MST audio-video and USB3.1 Gen2 data streams simultaneously. The input lane mapping is flexible and meets the USB Type-C connector flip orientation requirements. The incoming DP and USB signals are de-multiplexed, retimed, and transmitted on the Downstream Facing Ports (DFP). The MCDP52x0 consists of a USB DFP port with USB3.1 TX



Ordering Information

Part Number	Functional Description	Marking	Operating Temp.	Package	External Package
MCDP5200B0	USB-C to HDMI2.0/ USB-A (with retimer)	YYWWxxxxES	0°C to +70°C	TFBGA-169	TRAYS
MCDP5200B0T					Tape & Reel
MCDP5240B0	USB-C to DP++/ USB-A (with retimer)	YYWWxxxxES	0°C to +70°C	TFBGA-169	TRAYS
MCDP5240B0T					Tape & Reel
MCDP5250B0	DP1.4 to HDMI2.0	YYWWxxxxES	0°C to +70°C	TFBGA-169	TRAYS
MCDP5250B0T					Tape & Reel
MCDP5290B0	DP1.4 to DP++	YYWWxxxxES	0°C to +70°C	TFBGA-169	TRAYS
MCDP5290B0T					Tape & Reel

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and RX pair and an audio-video DFP port which can be configured as AC coupled DP/DP++ or DC coupled HDMI/DVI port, each with four high-speed lanes.

The combo receiver in MCDP52x0 supports all DP standard data rates up to HBR3 (8.1Gbps/lane) and USB3.1 Gen1 (5.0Gbps) and Gen2 (10.0Gbps). The dual mode (DP++) transmitter support DP standard data formats up to 8.1Gbps/lane or TMDS data format up to 6.0Gbps/lane. The side-band channel uses 1.0 Mbps Manchester-coded AUX signaling for DP and DDC signaling up to 100 kbps for the HDMI interface.

In the protocol converter mode, MCDP52x0 translates a DP SST stream into DC coupled HDMI2.0b output. The highest video timing supported in this mode is 4k2k60Hz RGB/YCC 444 or 4k2k120Hz in YCC 420 pixel format. It supports both RGB 444 and YCC444/422/420 video pixel encoding formats with a color depth up to 16 bpc (bits per component or 48 bits per pixel). The MCDP52x0 also has a pixel processing unit capable of video color space conversion from RGB444 to YCC444 with bit depth expansion and pixel encoding format conversion from YCC444 to YCC422/420. It also supports advanced dithering function to truncate the pixel bit depth to the precision of the connected sink device. Pixel format conversion along with horizontal blanking expansion improves interoperability and smooth rendering of video from mobile PC and tablets on legacy TVs. Besides, MCDP52x0 also supports HDMI CEC tunneling over DP AUX channel for remote control pass-through, one touch control of the connected devices in a CE system.

The MCDP52x0 processes High Dynamic Range (HDR) video content specified in BT601, BT709, BT2020 or in the Adobe RGB colorimetry format with the appropriate metadata conversion from DP to HDMI standard. It also offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.x or HDCP2.x content protection. MCDP52x0 functions as an HDCP1.x and HDCP2.x repeater between the DP source and DP or HDMI sink.

The MCDP52x0 can pass through DP SST or MST uncompressed streams with the flexibility of lane count and link rate conversion. The highest video timing per stream and the number of streams transported is limited by the DP1.4a link bandwidth.

The MCDP52x0 uses an external crystal of 25MHz as a reference clock for its operation. It has a 300MHz ARM Cortex M3 CPU with on-chip memories for storing data and code execution. The peripheral subsystem includes SPI, UART (debug only), and I2C master and slave interfaces. An internal Power-On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The MCDP52x0 uses an external 16Mbit SPI flash memory for storing the RSA-2048 signed application firmware with fail-safe recovery. At boot up, the CPU goes through a secure boot process authenticating the application code image stored in the SPI flash. It supports both standard mode and quad mode operation. A firmware update of the SPI flash is done securely through the DP AUX_CH or I2C host interface (Secure In-System-Programming).